EFFICIENT INSTRUCTION PREFETCH MECHANISM FOR DIGITAL SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

ABSTRACT OF THE DISCLOSURE

For use in a processor having an external memory interface, an instruction prefetch mechanism, a method of prefetching instructions and a digital signal processor incorporating the mechanism or the method. In one embodiment, the mechanism includes: (1) a branch predictor that predicts whether a branch is to be taken, (2) prefetch circuitry, coupled to the branch predictor, that prefetches instructions associated with the branch via the external memory interface if the branch is taken and prefetches sequential instructions via the external memory interface if the branch is not taken and (3) a loop recognizer, coupled to the prefetch circuitry, that determines whether a loop is present in fetched instructions and reinstates a validity of instructions in the loop and prevents the prefetch circuitry from prefetching instructions outside of the loop until the loop completes execution.